Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTION:**

1. **A**
2. **B**
3. **C**
4. **D**
5. **E**
6. **F**
7. **G**
8. **GND**
9. **Y**
10. **H**
11. **I**
12. **J**
13. **K**
14. **L**
15. **N. OC**
16. **VCC**

**.049”**

**3**

**4**

**5**

**6 7 8 9 10**

**13**

**12**

**11**

**2 1 16 15 14**

**MASK REF**

**S134**

**B**

**.039”**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004” X .004”**

**Backside Potential:**

**Mask Ref: S134 B**

**APPROVED BY: DK DIE SIZE .039” X .049” DATE: 5/25/21**

**MFG: TEXAS INSTRUMENTS THICKNESS .011” P/N: 54S134**

**DG 10.1.2**

#### Rev B, 7/19/02